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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,076	11/19/2003	Albert Cosand	03-0030	1075

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EXAMINER
BOLOURCHI, NADER

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
09/21/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/707,076	COSAND ET AL.	
	Examiner	Art Unit	
	Nader Bolourchi	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/9/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 2/20/2004 have been considered and made of record by the examiner.

Claim Rejections - 35 USC § 112

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 23, 26, 27 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: transimpedance amplifier to convert the clock signal and pulse-position modulated signal into voltage swing type signal for analog processing using time integrators.

Claims 2-22, 24-25, 28-37, and 39-40 are rejected due to their dependency to rejected claims 1, 23, 26, 27 and 38.

3. Claims 1 recites "a plurality of time integrators gated to generate a plurality of time-integrated signals in response to said at least one pulse-position modulated signal and said plurality of coordinating clock signals" (lines 6-9), which term "time integrators" makes it vague and unclear. It is not clear what term "time integrators" is referring to. Is it an integrator as disclosed in Fig. 4:78? If yes, then how its input could be a clock signal or Pulse-position modulated signal, rather than a voltage swing type signal for the propose of integration? The same rejection also stands for claims 23, 26, 27 and 38

Claims 2-22, 24-25, 28-37, and 39-40 are rejected due to their dependency to rejected claims 1, 23, 26, 27 and 38.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 23, 26, 27 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohtani (US 5,691,665).

Regarding claim 1, Ohtani discloses a data receiver (Fig. 1: 31) receiving at least one pulse-position modulated signal (Fig. 1: 41); a clock circuit (Fig. 1: 11 and Fig. 3) separating a reference clock signal (Fig. 1:42; Fig. 2:42) into a plurality of coordinating

clock signals (clock inputs of 121, 122, ... in Fig 3); a plurality of time integrators gated (Fig. 3: 121, 122, ... ; Examiner notes that all components of Holding unit 12 in Fig. 3 are gated by integration of their clock) to generate a plurality of time-integrated signals (SAMPLE [0], SAMPLE [1], ...) in response to said at least one pulse-position modulated signal (Fig. 3: 21) and said plurality of coordinating clock signals; and a combiner forming a demodulated signal from said plurality of time-integrated signals (Fig. 1: 34).

Regarding claim 23, Ohtani discloses a transmitter generating at least one pulse-position modulated signal (Fig.1; Examiner notes that inherently there is at least one transmitter for receiver shown in Fig. 1); and a communication receiver (Fig. 1) comprising; a data receiver (Fig. 1: 31) receiving said at least one pulse-position modulated signal (Fig. 1: 41); a clock circuit (Fig. 1: 11 and Fig. 3) separating a reference clock signal (Fig. 1:42; Fig. 2:42) into a plurality of coordinating clock signals (clock inputs of 121, 122, ... in Fig 3); a plurality of time integrators gated (Fig. 3: 121, 122, ... ; Examiner notes that all components of Holding unit 12 in Fig. 3 are gated by integration of their clock) to generate a plurality of time-integrated signals (SAMPLE [0], SAMPLE [1], ...) in response to said at least one pulse-position modulated signal (Fig. 3: 21) and said plurality of coordinating clock signals; and a combiner forming a demodulated signal from said plurality of time-integrated signals (Fig. 1: 34).

Regarding claim 26, Ohtani discloses a first station having a transmitter generating at least one pulse-position modulated signal (Fig.1; Examiner notes that inherently there is at least one station with transmitter for an station with a receiver shown in Fig. 1);; and a second station having a communication receiver (Fig. 1) comprising; a data receiver (Fig. 1: 31) receiving said at least one pulse-position modulated signal (Fig. 1: 41); a clock circuit (Fig. 1: 11 and Fig. 3) separating a reference clock signal (Fig. 1:42; Fig. 2:42) into a plurality of coordinating clock signals (clock inputs of 121, 122, ... in Fig 3); a plurality of time integrators gated (Fig. 3: 121, 122, ... ; Examiner notes that all components of Holding unit 12 in Fig. 3 are gated by integration of their clock) to generate a plurality of time-integrated signals (SAMPLE [0], SAMPLE [1], ...) in response to said at least one pulse-position modulated signal (Fig. 3: 21) and said plurality of coordinating clock signals; and a combiner forming a demodulated signal from said plurality of time-integrated signals (Fig. 1: 34).

Regarding claim 27, Ohtani discloses receiving at least one pulse-position modulated signal (Fig. 1: 41); separating a reference clock signal (Fig. 1:42; Fig. 2:42) into a plurality of clock signals (clock inputs of 121, 122, ... in Fig 3); gating a plurality of time integrators (Fig. 3: 121, 122, ... ; Examiner notes that all components of Holding unit 12 in Fig. 3 are gated by integration of their clock) to generate a plurality of time-integrated signals (SAMPLE [0], SAMPLE [1], ...) in response to said at least one pulse-position modulated signal (Fig. 3: 21) and said plurality of clock signals; and generating a demodulated signal from said plurality of time-integrated signals (output of Fig. 1: 34).

Regarding claim 38, Ohtani discloses receiving at least one pulse-position modulated signal (Fig. 1: 41); separating a reference clock signal (Fig. 1:42; Fig. 2:42) into a plurality of clock signals (clock inputs of 121, 122, ... in Fig 3); gating a plurality of time integrators (Fig. 3: 121, 122, ... ; Examiner notes that all components of Holding unit 12 in Fig. 3 are gated by integration of their clock) to generate a plurality of time-integrated signals (SAMPLE [0], SAMPLE [1], ...) comprising; beginning integration in response to the plurality of coordinating clock signals (SAMPLE [0], SAMPLE [1], ... are generated in response to clock inputs of 121, 122, ... in Fig 3); integrating a constant value (Fig. 12: VCC at the input of 131); and ceasing integration in response to said at least one pulse-position modulated signal (if PPM Signal 21 goes low, 131 is not clocked, and its operation is ceased); and generating a demodulated signal from said plurality of time-integrated signals (output of Fig. 1: 34).

Remarks

5. No claim is allowed.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dress et al. (US 2003/0235246 A1); Cosand et al. (US 2005/0105606 A1); and Devon et al. (US 5,684,871 A) which discloses that gated integrator is used with pulse-position modulation to maximize the signal to noise ratio.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nader Bolourchi whose telephone number is (571) 272-8064. The examiner can normally be reached on M-F 8:30 to 4:30.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David. C. Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

Nader Bolourchi
NB
09/07/2007

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER